JFLEX™

Specification

Document Revision 1.5

kontron

Contents

1. User Information

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2. Introduction

2.1 JFLEX™ Extension Module Concept

The JFLEX™ Extension Module Concept was specified for the use with the JRex SBC product line of Kontron Embedded Modules GmbH. JRex embedded line modules are characterized by the same surface pin-outs and interfaces for Reset/ATX feature, 2xUSB, FAST LAN, PS/2 Keyboard/Mouse connector, Compact-Flash socket, VGA and one serial port. These embedded line family features allow the use of the same chassis over the whole product line and maximize design reuse.

JRex embedded line modules allow the use of standard desktop memories and full ATX power supplies. An optional 5V-only version is available, too.

These homogeneous features facilitate easy upgrades within the JRex embedded line product family. Connection of displays is simplified when using the onboard standard JILI-Interface (JUMPtec® Intelligent LVDS Interface). JILI automatically recognizes which display is connected and independently sets all video parameters. All JRexes in the embedded line are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all JRex embedded line modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS of the SBC modules. This interface enables hardware independent access to the JRex features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight and user bytes in the EEPROM can be configured with ease by taking advantage of this standard JRex module feature.

The JRex embedded line products support the patented JFLEX™ extension module concept. A variety of JFLEX™ modules are available to extend the standard functionality of your JRex CPU board. The JFLEX extension bus is an open standard specified in this document.

General JRex and JFLEX™ information is obtained here:

JRex products

You can find a variety of existing JFLEX™ extension modules here:

JFLEX™ IO extensions

2.2 Overview of JFLEX™ Interfaces

JFLEX™ is a bus system with integrated extension interfaces to support additional functions with JRex products of Kontron Embedded Modules GmbH.

The bus provides the following subsystems:

- PCI Bus for additional PCI devices
- LPC Bus for more I/O devices
- AC97/MC97 Bus for sound features or modem functions (only one of them possible)
- serial interface with TTL signal levels
- infrared interface
- SMBus
- I2C Bus
- USB interface
- interface for a TV out module
- interface for a DVI output module
- digital panel interface with panel power sequence signals (*)
- LVDS panel output (*)
- Power signals

Notes:	(*) These functions depend on the JRex CPU board's capabilities.

There is not a must of a JFLEX™ extension module to support all JRex CPU modules and there is not a must for every CPU module to support every JFLEX extension module and every subsystem mentioned above.

Please consult your supplier or the Kontron website to find the right match or contact technical support. There may also be the availability of several application solutions from other vendors than Kontron.

3. Mechanical Specifications

3.1 Board Dimensions

When designing a JFLEX™ extension module the board dimensions must not exceed the over all size shown in the following drawing. Take care not to place any components on the bottom side inside of the area marked in red, otherwise the components may collide with the connectors on the JRex CPU boards below your module.

It is allowed to design JFLEX™ extensions in a smaller shape as long as it does not exceed the outer boarders of the basic shape below. The JFLEX™ graphic connector is only required when those features will be used on your extension module.

3.2 Stacking Height

The general JFLEX™ stacking height is 16mm (630mil). This specification only takes care of such modules. However, a stacking height down to 11mm (433mil) in special custom specific applications could be possible, too.

3.3 Connector Types

The JRex CPU modules use two 120 pin connectors **Molex® 53627-1205**.

On the JFLEX extension board this connector is matching with **Molex® 52837-1209** (or 52901-1205 with cover for automatic placement) placed on the bottom side.

For datasheet, drawing an product specification of the connectors please have a look at the Molex website www.molex.com and search for „53837“ or „53627“ or ask your local Molex dealer for details.

3.4 Extension Module Types

3.4.1 Stacking Characteristics

JFLEX™ extension modules can be of two different types:

- Mid Module:
  - the board is equipped with the bottom and the top connectors
  - it can be used anywhere in the JFLEX™ stack
  - all signals have to be routed from the bottom to the top connector
  - the designer has to take care not to exceed the height specifications

- Top Module:
  - the board is equipped with the bottom connector only
  - it can only be used on top of a JFLEX™ stack
  - the designer is free with the height of components used on the top layer

The maximum height of components on a JFLEX™ extension module PCB is specified as follows:

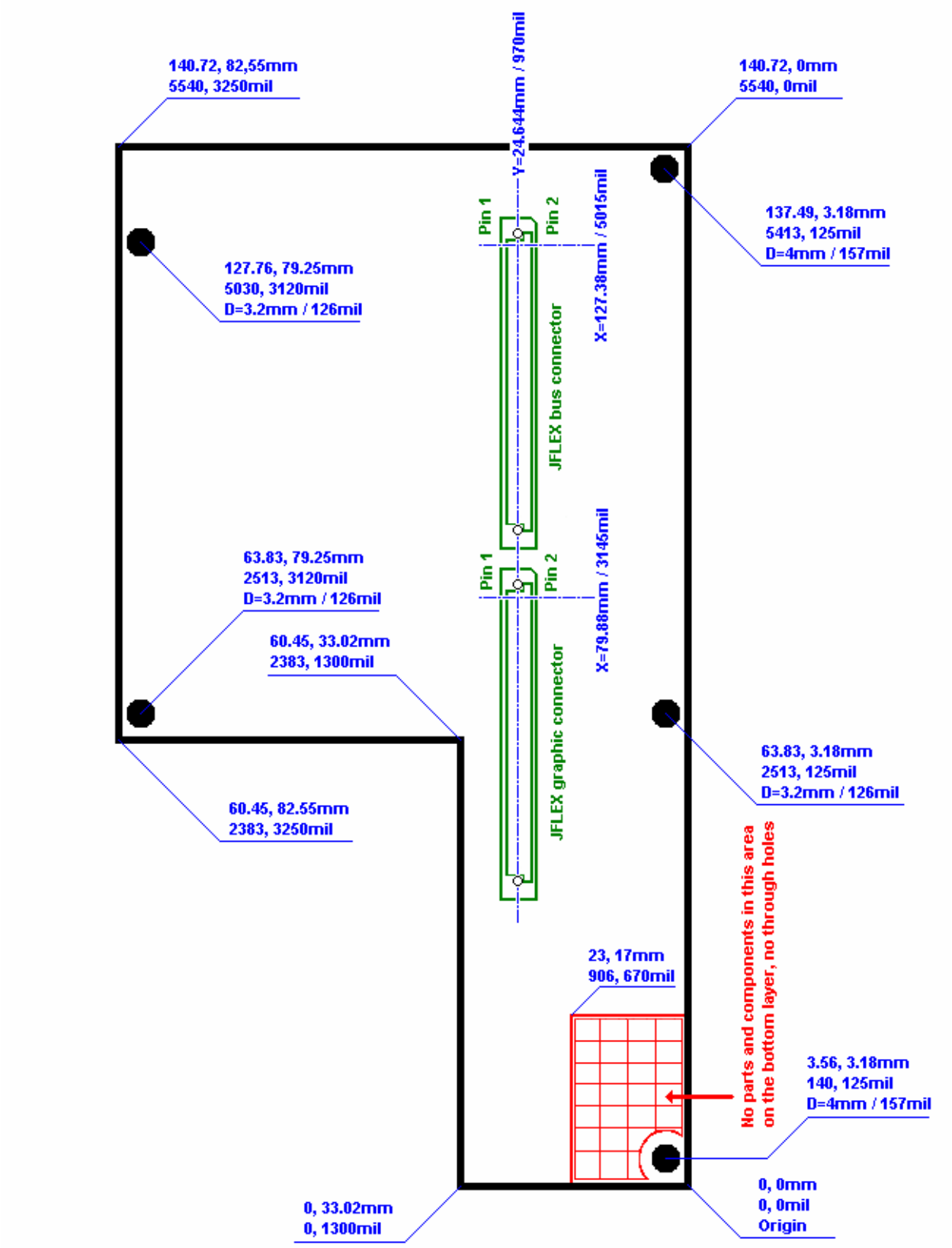
- bottom side: 3mm (118mil) for all boards
- top side: 12mm (472mil) for Mid Modules only

3.4.2 Functional Characteristics

The JFLEX bus concept is specified for up to 3 extension modules in the system. It may be possible under certain conditions to have more boards in the system, but the function of those configurations cannot be guaranteed.

The maximum number of extension boards with PCI function is limited to 2, i.e. the third module can only be a board with non-PCI function like LPC, Sound, etc. The extension modules with PCI function are referred to as First Stack Module and Second Stack Module. A Second Stack Module should not be equipped with a top PCI connector to avoid reflections and additional PCI load.

Notes:	The capability of supporting PCI functions depends on the CPU module's capabilities. There may be limitations due to the CPU modules PCI bus capabilities. Especially the number of available REQ/GNT signal pairs have to be considered here. See the CPU board manual for information.


140.72, 82,55mm
5540, 3250mil
Y=24.644mm / 970mil
140.72, 0mm
5540, 0mil
Pin 1
Pin 2
137.49, 3.18mm
5413, 125mil
D=4mm / 157mil
127.76, 79.25mm
5030, 3120mil
D=3.2mm / 126mil
X=127.38mm / 5015mil
JFLEX bus connector
63.83, 79.25mm
2513, 3120mil
D=3.2mm / 126mil
Pin 1
Pin 2
X=79.88mm / 3145mil
60.45, 33.02mm
2383, 1300mil
JFLEX graphic connector
63.83, 3.18mm
2513, 125mil
D=3.2mm / 126mil
60.45, 82.55mm
2383, 3250mil
No parts and components in this area
on the bottom layer, no through holes
23, 17mm
906, 670mil
3.56, 3.18mm
140, 125mil
D=4mm / 157mil
0, 33.02mm
0, 1300mil
0, 0mm
0, 0mil
Origin

3.5 JFLEX™ Bus Pin-Out

The following table shows the pin-out with signal names and the information to which subsystem the mentioned signal belongs.

Pin	Signal	Subsystem	Subsystem	Signal	Pin
1		Reserved	PCI	AD0	2
3	**3.3/0.5**	Power	PCI	AD1	4
5	LAD0	LPC	PCI	AD2	6
7	LAD1	LPC	PCI	AD3	8
9	LAD2	LPC	PCI	AD4	10
11	LAD3	LPC	PCI	AD5	12
13	LFRAME	LPC	PCI	AD6	14
15	LDRQ	LPC	PCI	AD7	16
17	LPCPD	LPC	PCI	CBE0	18
19	SERIRQ	LPC	PCI	AD8	20
21	IRQ10	LPC	PCI	AD9	22
23	IRQ11	LPC	PCI	AD10	24
25	**3.3/0.5**	Power	PCI	AD11	26
27	**GND**	Power	PCI	AD12	28
29	**3.3/0.5**	Power	PCI	AD13	30
31	RI	COM 2	PCI	AD14	32
33	DTR	COM 2	PCI	AD15	34
35	CTS	COM 2	PCI	CBE1	36
37	SOUT	COM 2	PCI	PAR	38
39	RTS	COM 2	PCI	SERR	40
41	SIN	COM 2	PCI	PERR	42
43	DSR	COM 2	PCI	LOCK	44
45	RSD	COM 2	PCI	STOP	46
47	**GND**	Power	PCI	DEVSEL	48
49	AC97CLK	AC97	PCI	TRDY	50
51	**3.3/0.5**	Power	PCI	IRDY	52
53	SDATA_OUT	AC97	PCI	FRAME	54
55	BITCLK	AC97	PCI	CBE2	56
57	SDATA_IN	AC97	PCI	AD16	58
59	SYNC	AC97	PCI	AD17	60
61	**GND**	Power	PCI	AD18	62
63	**3.3/0.5**	Power	PCI	AD19	64
65	EXTSMI	SM	PCI	AD20	66
67	CLKRUN	SM	PCI	AD21	68
69	PME	SM	PCI	AD22	70
71	SMBCLK	SM Bus	PCI	AD23	72
73	SMBDAT	SM Bus	PCI	CBE3	74
75	**GND**	Power	PCI	AD24	76
77	**5V**	Power	PCI	AD25	78
79	USB_OC	USB	PCI	AD26	80
81	USBa+	USB	PCI	AD27	82
83	USBa-	USB	PCI	AD28	84
85	**GND**	Power	PCI	AD29	86
87	**5V**	Power	PCI	AD30	88
89	USBb+	USB	PCI	AD31	90
91	USBb-	USB	PCI	REQ0	92
93	**GND**	Power	PCI	GNT0	94
95	**3.3/0.5**	Power	PCI	REQ1	96
97	I2DAT	I2C Bus	PCI	GNT1	98
99	I2CLK	I2C Bus	PCI	REQ2	100
101	ATXPWRGD	SM	PCI	GNT2	102
103	**GND**	Power	Power	**5V**	104
105	OSC	CLK	PCI	PCICLK	106
107	**3.3/0.5**	Power	Power	**GND**	108
109	IRTX	IR	PCI	PCIRST	110
111	**GND**	Power	PCI	INTD	112
113	IRRX	IR	PCI	INTC	114
115	**5V_SB**	Power	PCI	INTB	116
117	IRRXH	IR	PCI	INTA	118
119		Reserved	Power	**12V**	120

3.6 JFLEX™ Graphic Connector

This second connector provides additional graphic functions offered by the chipset of the used JRex CPU board like:

- TVout
- DVI interface
- secondary LVDS panel interface
- digital panel interface

As the capability and the implementation of those special graphic features vary from CPU board to CPU board, there is no standardized pin-out of this connector. Each JRex CPU board may have a different pin-out besides the power pins. A designer intending to use those features should understand that his JFLEX™ extension module would therefore be suitable for one JRex CPU board only.

Especially the TVout function will only be available with additional circuitry and needs different reference voltages for different chipsets.

We decided not to describe this graphic connector in this specification to avoid misunderstandings and wrong usage which may lead to damage of the CPU module and the JFLEX™ extension board.

Please contact your support channel to get hardware and BIOS information for your JRex in cases you want to use this graphic connector with one special JRex CPU board.

4. Electrical Specifications

This JFLEX™ specification is not a replacement for general guidelines concerning designs on the available buses and interfaces. Refer to the corresponding special design guidelines of chipset manufacturers, specifications for bus systems and interface specifications for details. If you don't know where to find those documents see the chapter Appendix A: Further Information Sources, too.

This document will only focus on issues that are different or need to be known for your special JFLEX™ design.

Every supplier of own JFLEX™ designs has to take care to fulfill the standards and legal requirements that apply.

4.1 Power Design Guidelines

JFLEX™ extension modules need to obtain power from the system. They are usually used on top of a JRex CPU module. Therefore the used power supply must be suitable to meet the requirements of the whole system. When choosing a power supply make sure it fulfills the specifications of the JRex CPU board you use and additionally make sure it is powerful enough to supply your whole system with all peripherals and components. Besides these general considerations, there are some special ones for the JFLEX™ extension module design. The intention of most designers is to use the power pins on the JFLEX™ bus connectors to supply their hardware. There are a few aspects to take care of which depend on the JRex CPU board in use. JRex CPU boards are available in two different versions, with ATX power connector and with AT (5V-only) power connector.

4.1.1 JRex CPU board with ATX power supply

If your JFLEX™ extension module is designed for the use with JRex CPU boards and an ATX power supply, only, a limitation results from the JFLEX™ connector. Each power pin on the connector allows a maximum current of 0.5A. Therefore all JFLEX™ modules in your system are not allowed to exceed the following maximum current values from the voltage lines that directly come from the ATX power supply:

Supply Voltage	JFLEX bus connector only		JFLEX Bus connector and JFLEX graphic connector	
3.3 V	7 pins	3.5A	7 pins	3.5A
5 V	3 pins	1.5A	6 pins	3.0A
12 V	1 pin	0.5A	7 pins	3.5A
5V Standby	1 pin	0.5A	1 pin	0.5A

WARNING	Make sure all your JFLEX™ extension modules don't exceed this absolute maximum values, if you only supply through the JFLEX™ connector. If power consumption is higher provide additional power connectors on your extension module to supply separately.

4.1.2 JRex CPU board with AT (5V-only) power supply

Most JRex CPU boards additionally are available as AT-versions. Contrary to the ATX-version the AT-version generates the 3.3V with help of an onboard DC/DC-converter. The DC/DC-converter serves onboard 3.3V components as well as the JFLEX™ connector's power pins. Of course such a voltage supply is no full replacement for an external power supply. Therefore the maximum current on the 3.3V lines is far lower than with the ATX-version boards. This limitation depends on the capability of the used JRex CPU board. Refer to the corresponding technical manual of the used JRex CPU board for limitation information.

WARNING	When designing JFLEX™ extension modules for and using them on JRex CPU boards in AT-version, make sure you don't exceed the maximum current values specified for that CPU board. Dragging more power will damage the onboard DC/DC-converter.

4.2 PCI Bus Routing Guidelines

The PCI 2.2 specification limits the maximum trace lengths for all 32-bit interface signals to 1.5 inches (3.81mm) for all expansion boards. On the JFLEX™ extension module things are a little different because they are used in a stack and they are expansion board and backplane together. The special requirements are described below. Nevertheless, for impedance control of all signals please follow the PCI 2.2 specification.

The chapter Functional Characteristics already informed that only two JFLEX™ extension modules with PCI-function are supported in the system. The following chapters describe the requirements for first stack and second stack extension modules.

4.2.1 First Stack Extension Modules

The first JFLEX™ extension module slot supports up to 3 additional PCI devices as standard. If three PCI devices are planed on your design, two of them have the PCI bus mastering capability and the third one should be a device without bus mastering. For compatibility reasons Kontron will give no support for not recommended designs with three PCI bus masters on the first extension slot.

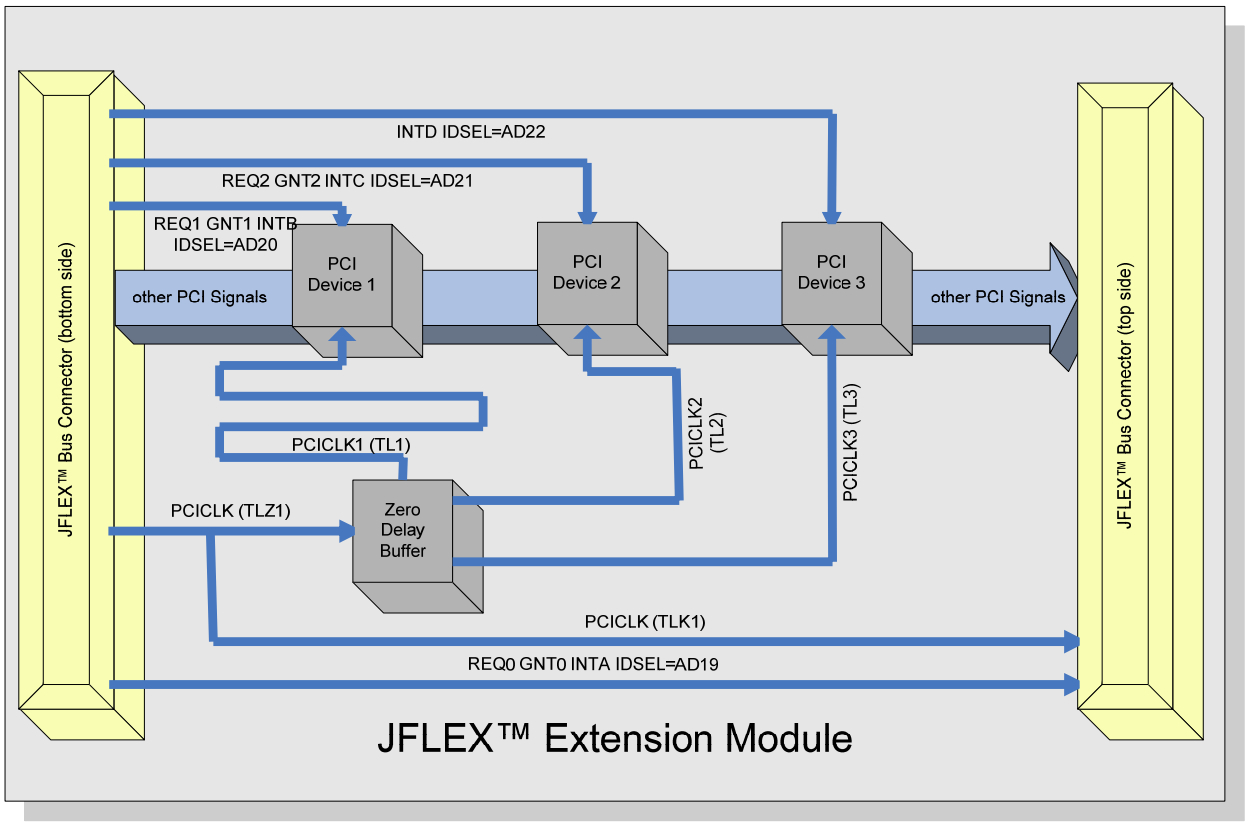
The third bus master channel is meant for the use of a second extension slot module.

It is also possible to extend the limited bus master capabilities of some chipsets with help of an additional CPLD device. Information about this CPLD solution can be requested from our technical support.

For more PCI devices a PCI-to-PCI bridge design is required. Those more complex designs are not focus of this specification.

Notes:	Not all JRex CPU modules support 3 PCI DMA channels. Designers have to check first if the JRex they intend to use offers enough REQ/GNT pairs for their design. See the technical manual of the JRex CPU module for information.

The following block diagram gives an overview of the recommended design for a first stack JFLEX™ extension boards:



Explanations of the block diagram

The first PCI device has to use the signals REQ1, GNT1, INTB and IDSEL=AD20.

The second PCI device has to use the signals REQ2, GNT2, INTC and IDSEL=AD21.

The third PCI device has no bus mastering capability and uses INTD and IDSEL=AD22.

REQ0, GNT0, INT A and IDSEL=AD20 will be used for a Second Extension Board in the JFLEX™ stack.

PCI signal trace layout

The maximum trace lengths for all signals except „System Pins“, „Interrupt Pins“ and „JTAG Pins“ should be as short as possible and not exceed a maximum length of 8.0 inches (20.32cm). The routing of these signals should be “daisy chain” in order to reduce reflections.

PCI clock layout

It is recommended to use a Zero Delay Clock Buffer on the PCICLK signal. All clocks should have the same trace length of 3.0 ± 0.1 inch (7.62 ± 0.25cm) starting from the bottom side JFLEX™ bus connector and ending on the PCI device. The PCICLK routing from the bottom JFLEX™ connector to the top one has to be a direct connection (shortest trace length possible).

Definitions:

- TLZ1 = trace length from JFLEX™ connector to Zero Delay Buffer
- TL1 = trace length from Zero Delay Buffer to PCI Device 1 slot 1
- TL2 = trace length from Zero Delay Buffer to PCI Device 2 slot 1
- TL3 = trace length from Zero Delay Buffer to PCI Device 3 slot 1
- TLU1 = trace length from bottom side JFLEX™ connector to top side one

Trace length:

- TLZ1 + TL1 = 3.0 ± 0.1 inch
- TLZ1 + TL2 = 3.0 ± 0.1 inch
- TLZ1 + TL3 = 3.0 ± 0.1 inch
- TLU1 = 0 ± 0.1 inch

Example:

Assuming the TLZ1 of your design will be 1.0 inch the other trace lengths TL1, TL2 and TL3 all have to be 2.0 inch.

4.2.2 Second Stack Extension Modules

Modules designed for second stack JFLEX™ slot are not fully PCI2.2 compliant. Such a module is only specified for one additional PCI device.

PCI signal trace layout

The maximum trace lengths for all signals except „System Pins“, „Interrupt Pins“ and „JTAG Pins“ should be as short as possible and not exceed a maximum length of 1.4 inches (3.56cm). The routing of these signals should be “daisy chain” in order to reduce reflections.

PCI clock layout

As the PCICLK total trace length has to be 3.0 ± 0.1 inch (7.62 ± 0.25cm), too, and the following definitions are valid:

- TLC = trace length inside of the JFLEX™ connectors (0.63 inch or 16mm)
- TLZ2 = trace length from JFLEX™ connector to Zero Delay Buffer
- TL4 = trace length from Zero Delay Buffer to PCI Device 1 slot 2
- TLU1 = trace length from bottom side JFLEX™ connector to top side one slot 1 (0 inch)

Trace length:

- TLU1 + TLC + TLZ2 + TL4 = 3.0 ± 0.1 inch

Example:

Assuming the first stack module really has a TLU = 0 inch and the recommended standard connectors with TLC = 0.63 inch are used the total trace length on the second stack module has to be 2.36 ± 0.1 inch. Additionally knowing that TLZ2 is routed with a trace length of 2.0 inch, TL4 has to be 0.36 inch.

4.3 LPC Design Guidelines

Please check first whether the JRex CPU module you intend to use supports the LPC (Low Pin Count) bus and your LPC device.

The LPC bus is a serial I/O bus with a small amount of pins and can be used to substitute some I/O functions known from the ISA bus. It runs with the PCI frequency of 33MHz.

For the LCLK signal on your LPC I/O chip please use the PCI clock and follow the PCI clock layout guidelines. For the other signals please follow the PCI signal trace layout guidelines in the PCI Bus Routing Guidelines of this specification.

If you don't use the LPC signals on your design please leave them unconnected. No pullup resistors are required on the JFLEX™ extension module.

For further information on this bus please refer to Intel®'s Low Pin Count Interface Specification.

4.4 AC97/ MC97 Design Guidelines

Please check first whether the JRex CPU module you intend to use supports the AC97 feature and your codec.

The digital AC Link is working with 12.288 MHz. The JFLEX™ bus is just supporting a single Codec. The signal routing is not critical in terms of trace length.

If you are using the AC97 link just connect the codec to the necessary power and AC97 signals.

If you don't use the AC97 link leave the signals unconnected. There are no pullup resistors on your JFLEX™ module.

For further information please refer to Intel®'s Audio Codec 97 Specification.

4.5 Serial Interface Design Guidelines

Please check first whether the JRex CPU module you intend to use supports the additional serial interface.

You can either use the TTL signals directly or need to add a transceiver circuitry to your JFLEX™ design (e.g. RS232 or RS422/485) depending on the application requirements. Please refer to the corresponding transceiver datasheets for more information.

If you don't want to use this feature or only need a part of the serial interface signals, leave them unconnected. You don't need pullup resistors on your JFLEX™ design.

4.6 Infrared Interface Design Guidelines

Please check first whether the JRex CPU module you intend to use supports the IR feature.

If you want to use the IR signals of the JFLEX™ bus, just connect them with your IR module. To reduce the noise, make sure you are using a good power supply solution for this kind of applications. As the IR signals are not fast they are not critical in the layout.

If you don't intend to use the IR signals please leave them unconnected. There are no pullup resistors required on your JFLEX™ design.

4.7 SMBus and I2C Bus Design Guidelines

SMBus and I2C Bus are very similar. They are both serial buses with one clock and one data line. Devices connected to this bus usually have a hard-coded unique address for the communication with the host. If you intend to use one of these buses on your JFLEX™ board, designer has to take care only unused addresses in the system are hard-coded at the new device on the bus system.

The data and the clock line are not critical in trace length routing.

The SMBus signals are coming from a SMBus controller onboard of the JRex CPU board. Please refer to the SMBus Specification for more details.

The I2C Bus coming from the JRex CPU board is not served by an I2C bus controller. The communication is a BIOS software emulation done with the help of two I/O signals. Therefore it is not a complete I2C implementation. The CPU board itself is the only master on the bus and has to initiate the communication to the connected devices. This bus is only meant to be used with simple I2C storage devices. Other devices are not supported.

If you do not want to use these buses leave the signals unconnected. There are no pullup resistors required on your design.

For further information on I2C implementations refer to the I2C specification.

4.8 USB Interface Design Guidelines

Please check first whether the JRex CPU module you intend to use supports this additional USB interface.

If you want to use the USB interface signals connect the differential signals to your USB device. Make sure the power lines can supply the necessary current for your USB devices. As there is no resetable fuse on the power lines, this has to be added by the JFLEX™ extension board designer. The USB specification defines that a fuse has to be used and this measure will also protect your JRex CPU board to get damaged by a defective USB device. If you don't intend to use the USB interface leave the signals unconnected. There are no pullup resistors required on your JFLEX™ module.

For further information refer to the USB 2.0 specification.

5. Appendix A: Further Information Sources

The following sources of information can help you better understand PC architecture, buses and interface.

5.1 Buses

5.1.1 LPC Bus Information

- Intel® Low Pin Count Interface Specification, Revision 1.1, Intel® Corporation

5.1.2 PCI Bus Information

- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, which develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.

- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

5.1.3 SM Bus and I2C Bus Information

- I2C Bus Specification, Revision 2.1, Philips Semiconductors

- System Management Bus (SMBus) Specification, Revision 2.0, SBS Implementers Forum.

5.2 Interfaces

5.2.1 Serial RS-232 Interface

- EIA-232-E standard

The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

- National Semiconductor

The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

5.2.2 USB Interface

- USB Specification

The USB Implementers Forum (USB-IF) is a nonprofit corporation founded by the group of companies that developed the Universal Serial Bus specification. USB-IF provides a support organization and forum to advance and adopt Universal Serial Bus technology. You can search for information about the standard on the Web.

5.2.3 AC’97 Interface

- Intel® Audio Codec ‘97 Specification, Revision 2.3, Intel® Corporation

5.2.4 IrDA Interface

- IrDA Specification

The Infrared Data Association was founded by a group of well known companies that develop and maintain the ‘IrCOMM’ Serial and Parallel Port Emulation over IR. You can search the Web for more information.

5.3 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
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5.4 Programming

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- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

6. APPENDIX B: REVISION HISTORY

Revision	Date	Edited by	Changes
JFLEX101	05.08.2002	WKA	First release with PCI guide
JFLEX102	11.10.2002	WKA	Added mechanical data and pin-out
JFLEX103	07.02.2003	WKA	Changed pin 21 to ISA IRQ10 and pin 23 to ISA IRQ11
JFLEX104	26.03.2003	WKA	Erased error on JFLEX bus connector pin 119 and 120
JFLEX110	05.05.2003	WKA	First official release
JFLEX111	10.12.2003	WKA	Added restriction on the bottom side (collision with JRex USB)
JFLEX112	19.04.2004	WKA	Removed JFLEX graphic connector pin-out (not identical on PM)
JFLEX113	26.05.2004	WKA	Corrected mistake with upper and lower JFLEX bus connector p. 3
JFLEX114	04.05.2006	BAJ	Minor changes
JFLEX115	08.01.2007	BHO	Changed to Kontron style, added limitation information for JRex with 5V-only, reworked drawings and guidelines